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TITLE: A HIGH SPEED MEMORY INTERFACE SYSTEM AND METHOD

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USSN: 10/032,248

Attorney Docket #: CYPR-CD01080

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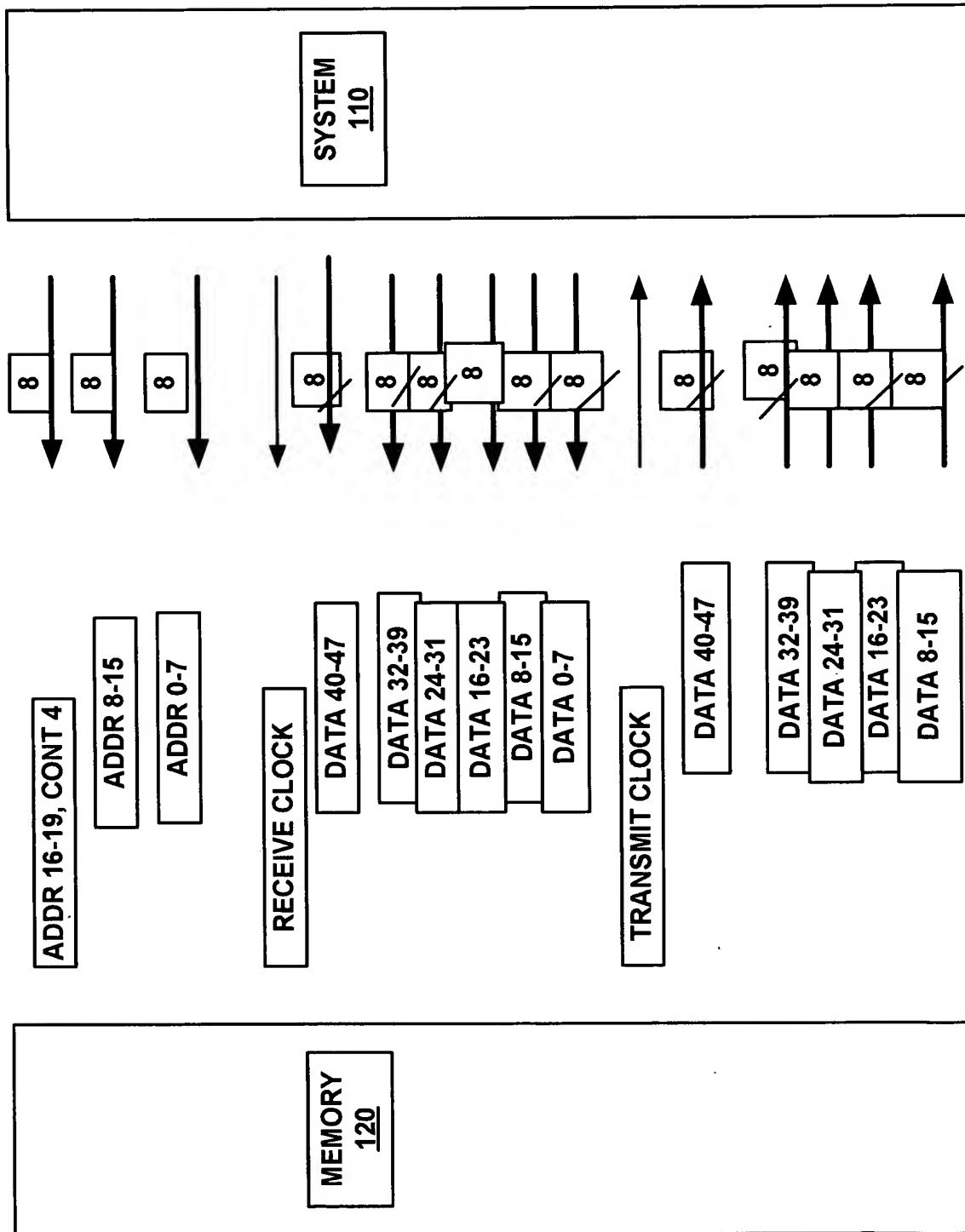


FIGURE 1 (PRIOR ART)

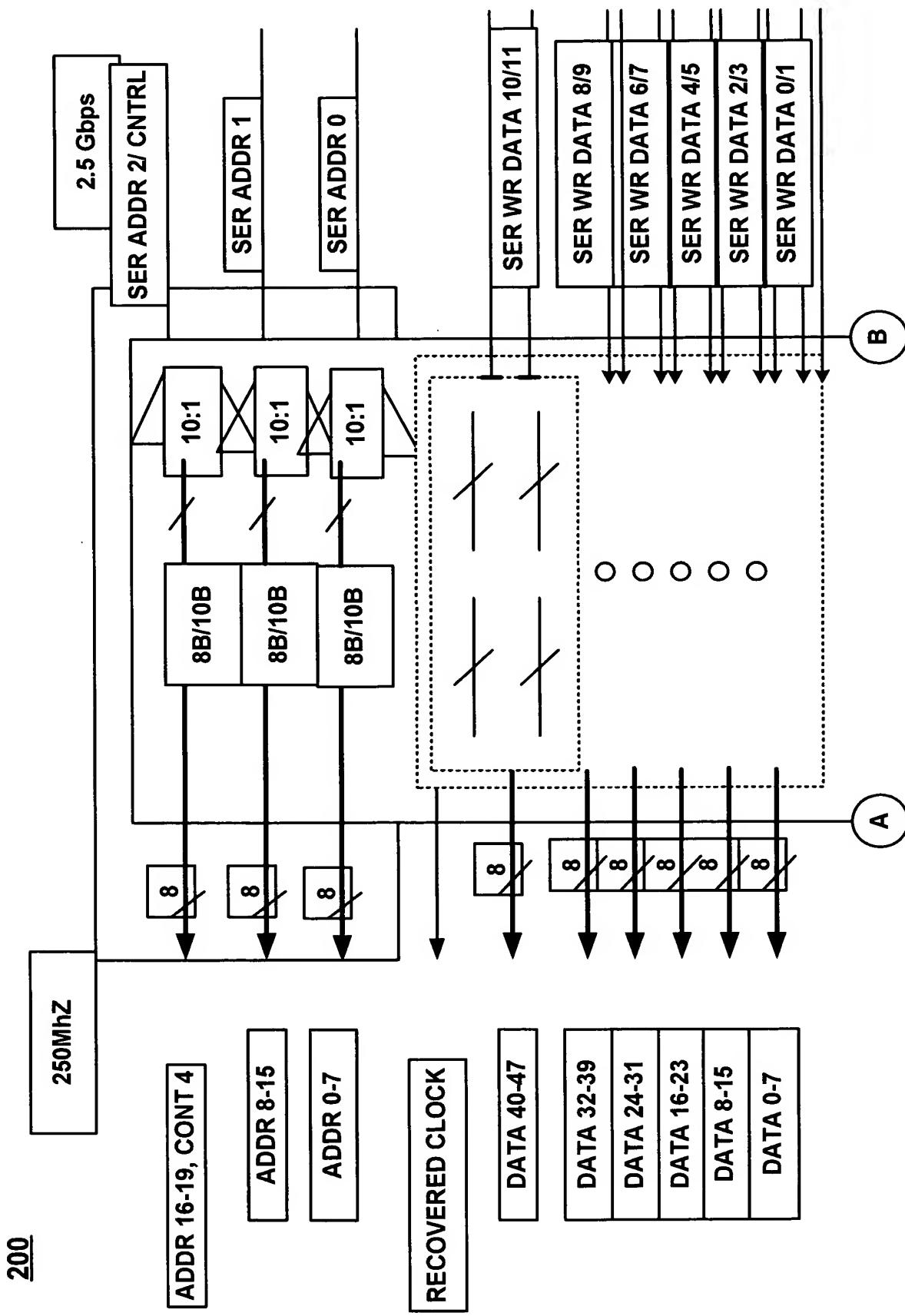


FIGURE 2

200 (CONT.)

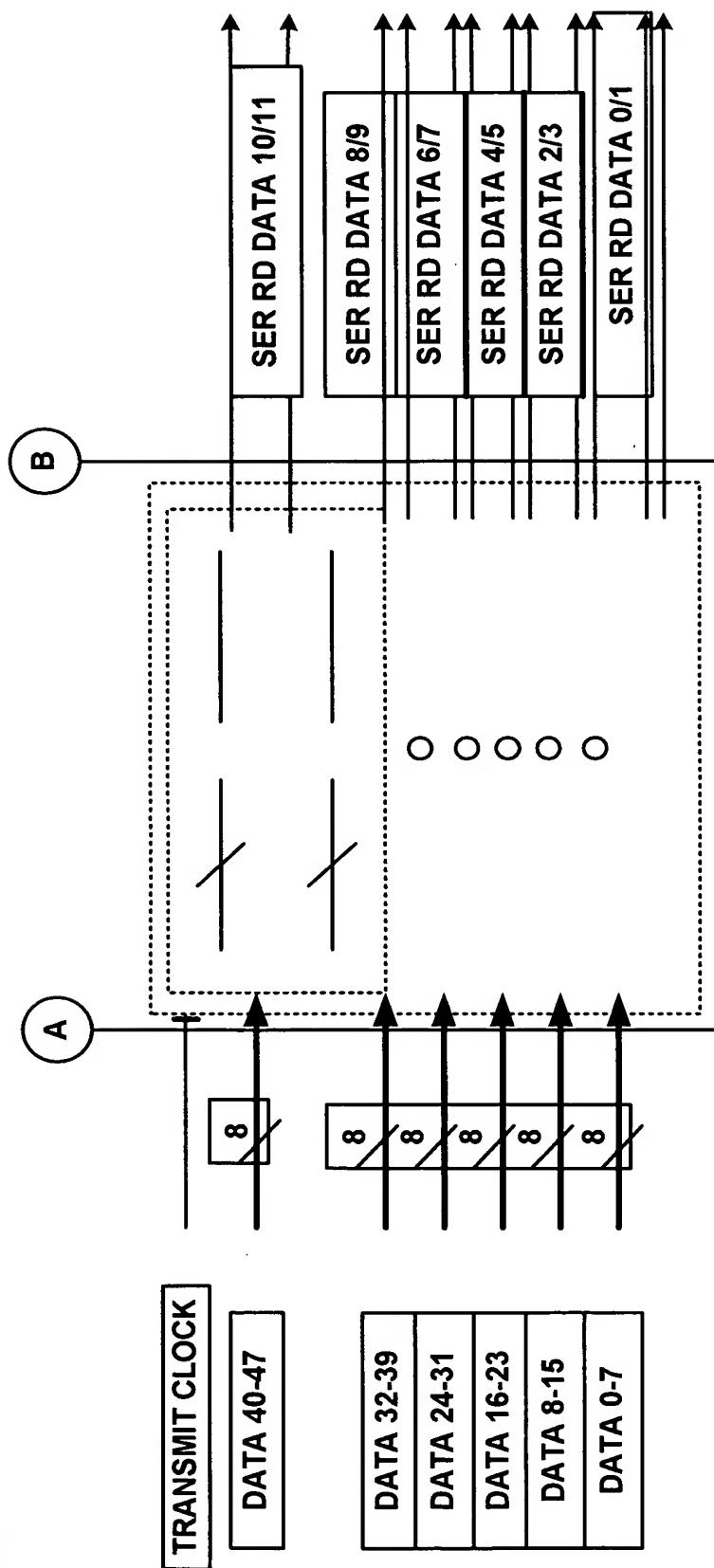
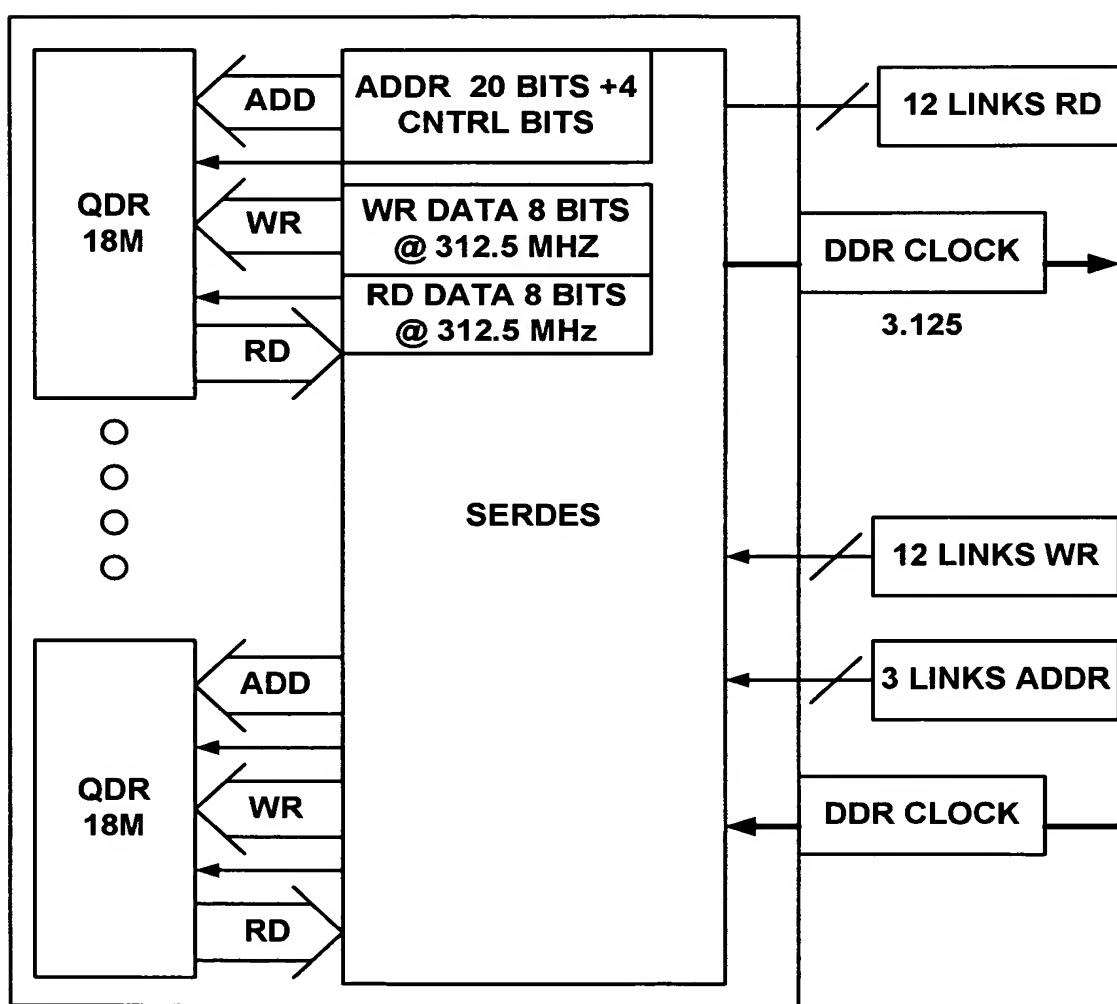


FIGURE 2 (CONT.)

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300**FIGURE 3**

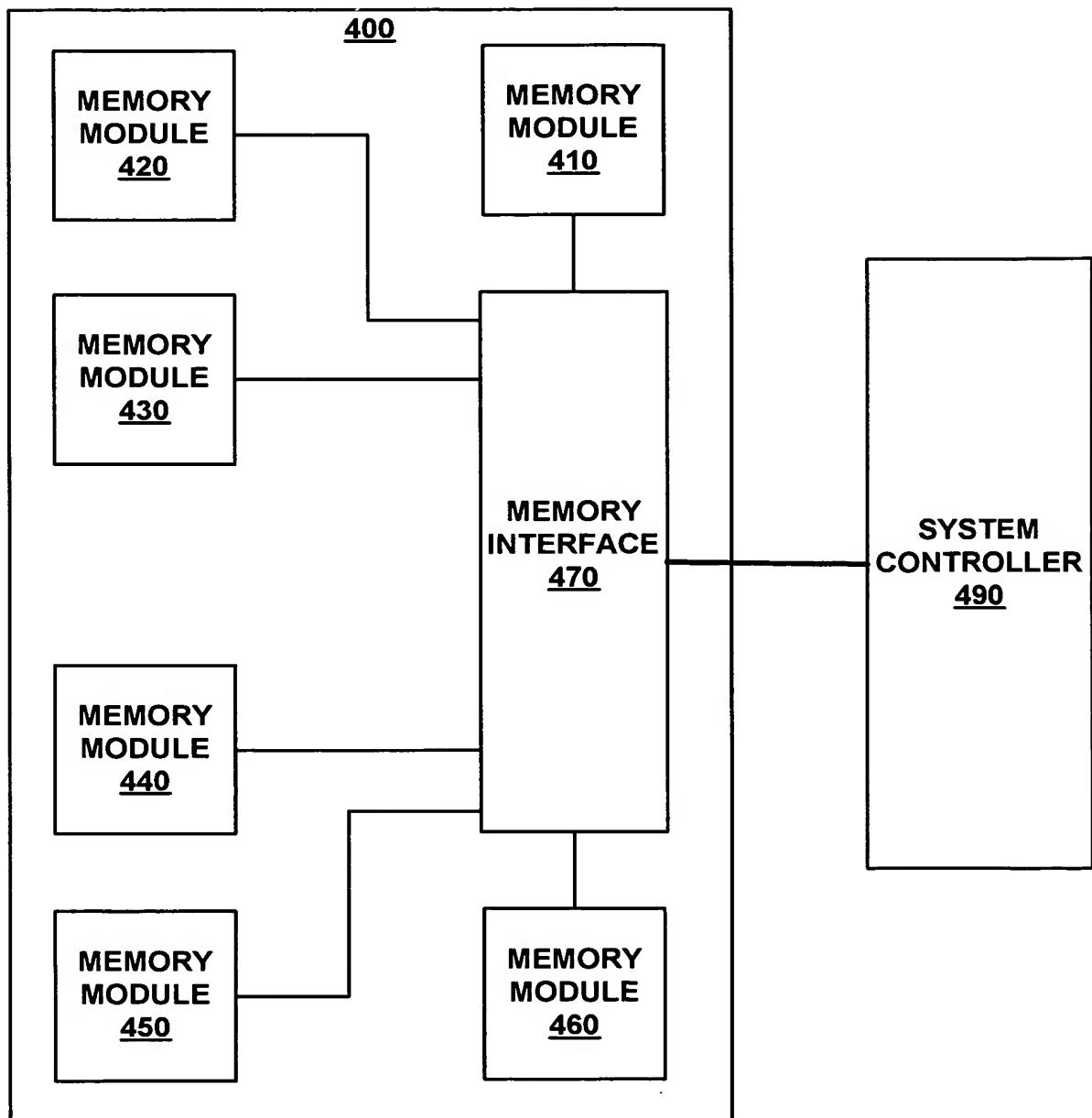


FIGURE 4

500

**ENGAGING IN SERIAL COMMUNICATIONS AT A FIRST RATE
WITH A SYSTEM MEMORY CONTROLLER.**

510

**EXECUTING PARALLEL COMMUNICATIONS WITH A
MEMORY ARRAY AT A SECOND RATE.**

520

**CONFIGURING THE INFORMATION IN PROPER ALIGNMENT
FOR COMMUNICATION BETWEEN SERIAL SYSTEM
CONTROLLER SIGNALS AND PARALLEL MEMORY ARRAY
SIGNALS.**

530

FIGURE 5

610

PHASE ALIGN SIGNALS ON A TRANSMIT CHANNEL

611

ENCODE SIGNALS ON THE TRANSMIT CHANNEL

612

SERIALIZE SIGNALS ON THE TRANSMIT CHANNEL

613

FIGURE 6A

620

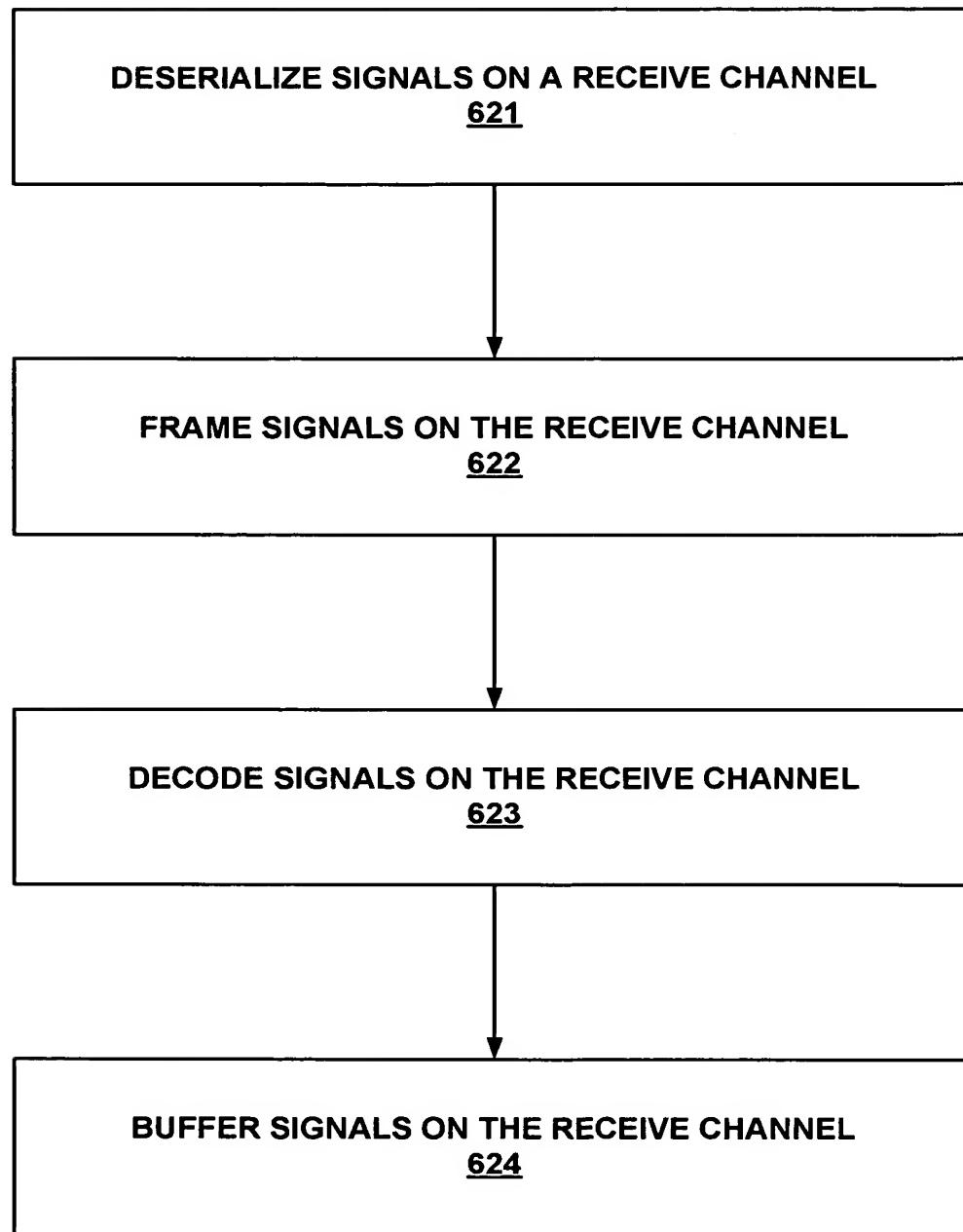


FIGURE 6B

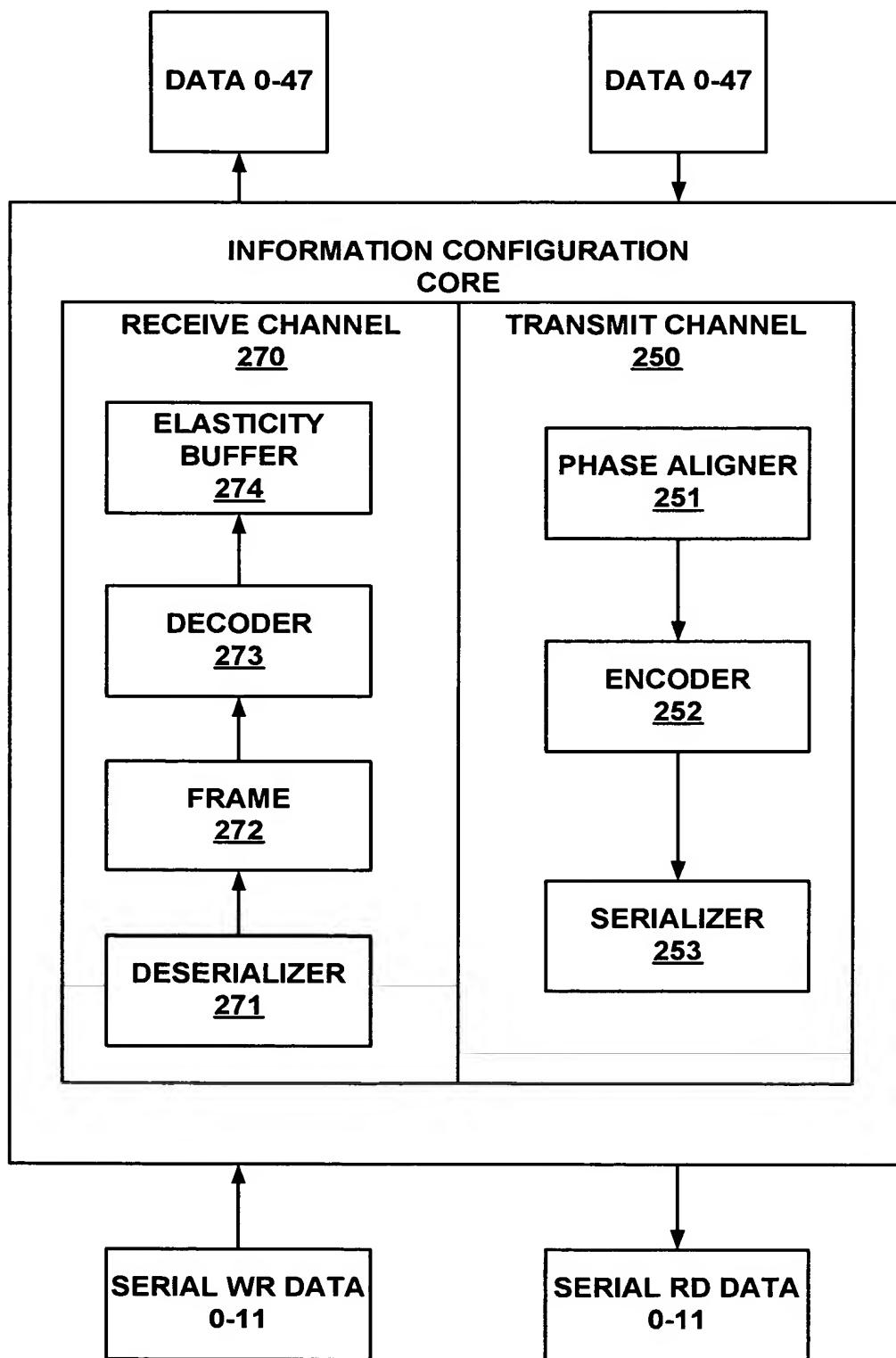


FIGURE 7

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